Source-Level Performance, Energy, Reliability, Power and Thermal (PERPT) Simulation

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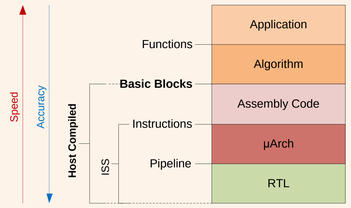
Introduction

Motivation

- Increasing design complexities
  - HW/SW co-design with multi-dimensional evaluation metrics
  - ➢ Rapid evaluation methods are desired
- Traditional simulation models
  - Instruction Set Simulator (ISS)
  - RTL/Gate level
  - ➢ Too slow or too inaccurate
- Modeling at higher abstraction levels
  - Fast and accurate
  - ➢ Host-compiled simulation



Source-level PERPT Modeling

- Modeling above ISS level
  - Compile and execute application natively
  - Annotate application with target timing, energy and reliability metrics
  - Online Architectural Vulnerability Factor (AVF) analysis
  - Generating power traces for thermal estimation

➢ Fast and accurate source-level simulation to complement ISS

Challenges & Solutions

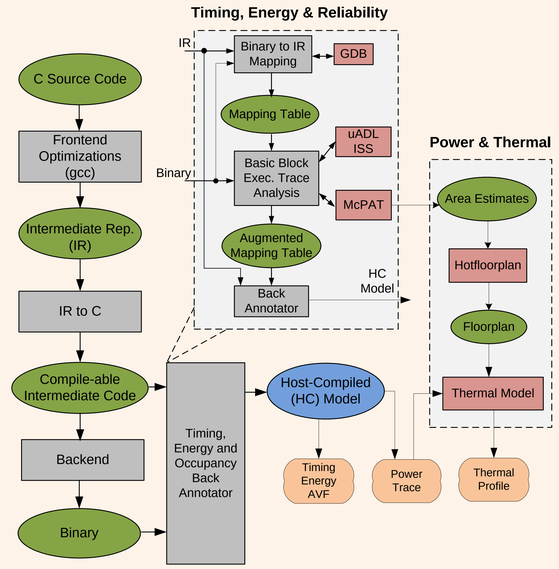
- Annotation granularity?
  - Speed vs. accuracy tradeoff
  - ➢ Block (BB) granularity
- Compiler optimizations?
  - Mapping between source and binary
  - ➢ Work with intermediate representation (IR)
  - ➢ Use IR and debug information to reconstruct memory traces
- Dynamic architecture effects?
  - Pairwise characterization to capture pipeline states
  - Lightweight cache model to capture dynamical memory behaviors

Retargetable Back Annotator

Retargetable PERPT Back-Annotation Flow

- Annotate at IR level
  - Consider front-end optimization
  - IR to C conversion for host execution
- Basic block timing, energy and reliability characterization
- Running back-to-back with power and thermal model

➢ Retargetable back annotator for PERPT simulation



Binary-to-IR Mapping

- Backend optimizations
  - Instruction scheduling
  - ➢ Control flow mismatches

➢ Graph matching heuristic
  - ➢ Synchronized depth-first traversal

- Memory trace reconstruction
  - Global and stack variables
  - ➢ Rely on debug information and IR analysis
  - ➢ Simulate stack pointer online

Basic Block Characterization

- Metrics depend on system state before BB entry
- Real execution approximated
  - Pairwise characterization with uADL ISS and McPAT
  - Inter-block stall or overlap is reflected in characterized block
  - Collect time stamps of accesses to micro-arch. structures for AVF modeling

Back-annotation into IR

- Target metrics back-annotation
  - Annotate timing, energy and reliability metrics
    - Perform AVF estimation by online producer-consumer analysis
    - Insert a lightweight cache model to capture memory related metrics
    - Generate power traces to drive thermal estimator (HotSpot, DTTEM)
- Path dependent metrics
  - Capture static branch predictors

➢ Source-level PERPT simulation model

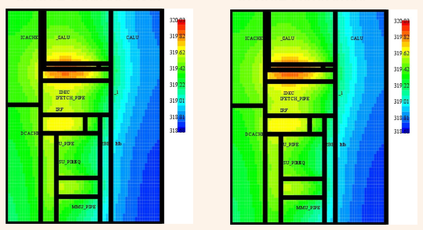
Experimental Results

Accuracy Results

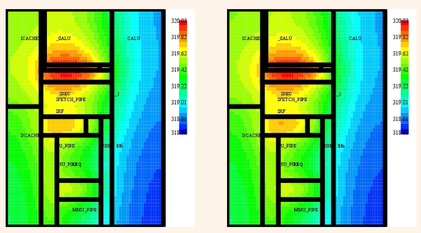
- Auto., office, network, security and telecomm. applications with small and large dataset [MiBench]
- Dual- (z6-like) and single-issue (z4-like) e200 PowerPC
  - 16KB 4-way associative caches
  - Static branch prediction, in-order pipeline
  - 500 MHz operating frequency
- Compare against cycle-accurate reference ISS+McPAT+HotSpot
  - ➢ >90% accuracy for timing, energy, reliability and power estimation
  - ➢ An Average of 0.05K exists in steady-state thermal estimation

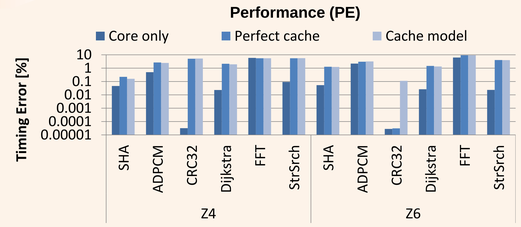
Thermal (PEPT)

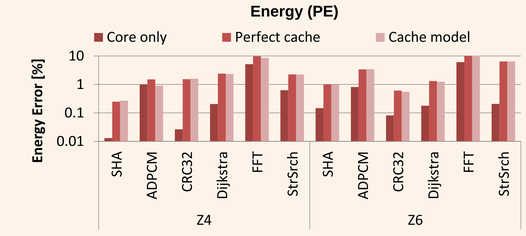
CRC32 Source level | CRC32 Reference

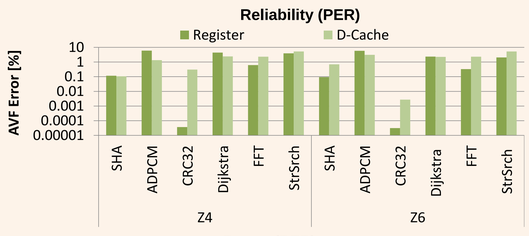


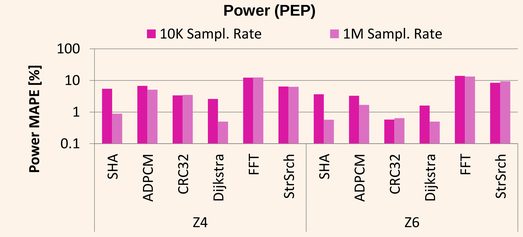
SHA Source level | SHA Reference





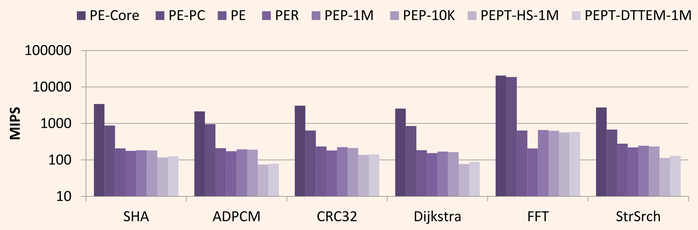


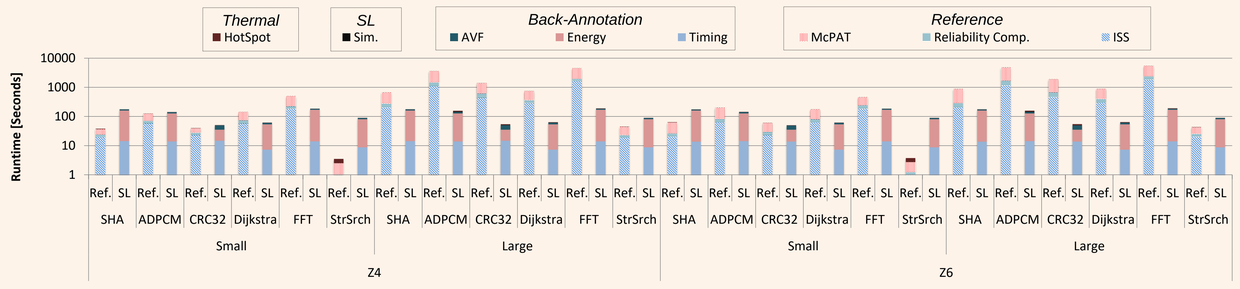




Speed Results

- One-time back-annotation
  - 3min. to 3s BA runtime
- Source-level simulation vs. traditional ISS
  - PE: 290MIPS - 5740MIPS at various abstract level
  - PER: 185MIPS for register file and D-cache AVF
  - PEP: 280MIPS at 1M sampling rate
  - PEPT: 180MIPS at !M sampling rate
  - Equivalent ISS @0.66MIPS
  - Source-level simulation runtime is 15-20 times faster that traditional cycle accurate ISS





Publications
[1] S. Chakravarty, Z. Zhao, A. Gerstlauer, "Automated, Retargetable Back-Annotation for Host-Compiled Performance and Power Modeling," CODES+ISSS, October 2013.
[2] D. Gandhi, A. Gerstlauer, L. John, "FastSpot: Host-Compiled Thermal Estimation for Early Design Space Exploration," ISQED, March 2014.
[3] Z. Zhao, A. Gerstlauer, L. John, "Source-Level Performance, Energy, Reliability, Power and Thermal (PERPT) Simulation," TCAD, pre-print, June 2016.